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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/782,743	02/13/2001	Howard E. Rhodes	303.592US1	9680

7590 06/03/2003

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EXAMINER
PHAM, LONG

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/782,743	RHODES, HOWARD E.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6,9,10,17,18,36,38 and 45-56 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6,9,10,17,18,36,38 and 45-56 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1 and 3, as written, taught, and understood, are rejected under 35 U.S.C. 102(a) as being anticipated by Liu (US '861).

Liu teaches a method comprising (see figures 1-6 and col. 1, line 20 to col. 4, line 35):

preparing a substrate 10, wherein preparing the substrate, comprising: forming a gate oxide layer 18; and forming a polysilicon layer 20; and forming one or more dual gate structure 30 or 32 using only mask 22.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 4, 45, 46, 47, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu (US '861) as applied to claims 1 and 3 above, and further in view of Gardner et al. (US '471).

Liu further teaches forming a first gate structure having a first conductivity in the substrate, the first gate structure 32 is being formed by an in-situ process, and forming a second gate structure 30 having a second conductivity in the substrate, the second conductivity having a different

value than the first conductivity, and the second gate structure being formed using only one masking operation.

Liu teaches forming the first gate structure 32 by an in-situ process, but fails to teach the first gate structure is formed by one blanket implantation as recited in present claim 4.

Gardner teaches a method for forming a CMOS device in which a doped polysilicon layer for forming gate structures is formed by blanket implantation. See figure 1A and col. 5, lines 25-40.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** form the first gate structure by blanket implantation because in doing so the use of masking is avoided.

Liu fails to teach forming a sacrificial oxide layer with a thickness on a semiconductor as recited in present claims 2 and 47.

However, the formation of a sacrificial oxide layer on a semiconductor is well-known to ***one of ordinary skill in the art of making semiconductor devices***.

Liu teaches forming the gate structures and a PWELL 12 on the substrate but fails to teach that the substrate is doped n-type as recited in present claim 45.

However, the formation of gate structures or MOS devices on a substrate of n-type or p-type conductivity is well-known to one skilled in the semiconductor art.

With respect to present claim 46, Liu further teaches that the dual gate structures are complementary metal-oxide- semiconductor dual gate structures. See figures 1-6 and associated text.

With respect to present claim 48, Liu further teaches that the gate oxide layer has a thickness of between 20-100 Angstroms.

5. Claims 5 and 6, as written, taught, and understood, are rejected under 35 U.S.C. 102(a) as being anticipated by Liu (US '861).

Liu teaches a method comprising (see figures 1-6 and col. 1, line 20 to col. 4, line 35):

preparing a substrate 10;

forming a first gate structure 32 including a P well 12 without a mask; and forming a second gate structure 30 including an N well 14 using only one mask, wherein forming a second gate structure including an N well 14 using only one mask comprises: forming a deep N well 14.

6. Claims 49, 50, 51, 52, 53, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu (US '861) as applied to claims 5 and 6 above, and further in view of Gardner et al. (US '471).

Liu teaches forming the gate structures and the PWELL 12 on the substrate but fails to teach that the substrate is doped n-type as recited in present claim 49.

However, the formation of gate structures or MOS devices on a substrate of n-type or p-type conductivity is well-known to one skilled in the semiconductor art.

Liu teaches forming the first gate structure 32 by an in-situ process, but fails to teach the first gate structure is formed by one blanket implantation as recited in present claim 50.

Gardner teaches a method for forming a CMOS device in which a doped polysilicon layer for forming gate structures is formed by blanket implantation. See figure 1A and col. 5, lines 25-40.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** form the first gate structure by blanket implantation because in doing so the use of masking is avoided.

Gardner fails to teach energy for the implantation as recited in present claims 50, 52, and 53.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the implantation energy through routine experimentation and optimization to obtain optimal or desired device performance because the implantation energy is a result-effective variable and there is no evidence indicating that the implantation energy is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Liu teaches forming the PWELL without using masking but fails to teach that the PWELL has a depth as recited in present claims 51, 52, and 54.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the depth of the PWELL through routine experimentation and optimization to obtain optimal or desired device performance because the depth of the PWELL is a result-effective variable and there is no evidence indicating that the depth of the PWELL is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Claim Rejections - 35 USC § 103

7. Claims 9, 10, and 55, as written, taught, and understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu (US '861).

Liu teaches a method comprising (see figures 1-6 and col. 1, line 20 to col. 4, line 35):

preparing a substrate 10;

forming a first gate structure 32 including a P well 12 without a mask; and forming a second gate structure 30 including an N well 14 using only one mask, wherein forming a second gate structure including an N well 14 using only one mask comprises: forming a deep N well 14.

Liu fails to teach the value for the depth of the P well as recited in present claim 9.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal value for the depth of the well through routine experimentation and optimization to obtain optimal or desired device performance because the depth of the well is a result-effective variable and there is no evidence indicating that claimed value is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Liu teaches forming the first and second gate structures on a substrate but fails to teach that the substrate is doped n-type as recited in present claim 54.

However, the formation of gate structures or MOS devices on a substrate of n-type or p-type conductivity is well-known to one skilled in the semiconductor art.

Claim Rejections - 35 USC § 103

8. Claims 17 and 18, as written, taught, and understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu (US '861).

Liu teaches a method comprising (see figures 1-6 and col. 1, line 20 to col. 4, line 35):

preparing a substrate 10;

forming a first gate structure 3; and

forming a second gate structure 30 including an N well 14 using only one mask.

Liu further teaches that the first gate structure is formed to have a first conductivity using in-situ process in the substrate but Liu fails to teach that the first conductivity is introduced into the first gate structure by one blanket implantation as recited in present claim 17.

Gardner teaches a method for forming a CMOS device in which a doped polysilicon layer for forming gate structures is formed by blanket implantation. See figure 1A and col. 5, lines 25-40.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** form the first gate structure by blanket implantation because in doing so the use of masking is avoided.

Liu teaches that the N well has a depth but fails to teach the depth value as recited in present claim 18.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal value for the depth of the N well through routine experimentation and optimization to obtain optimal or desired device performance because the depth of the N well is a result-effective variable and there is no evidence indicating that the depth of the N well is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

9. Claim 36, as written, taught, and understood, is rejected under 35 U.S.C. 102(a) as being anticipated by Liu (US '861).

Liu teaches a method comprising (see figures 1-6 and col. 1, line 20 to col. 4, line 35):

forming a first gate structure 32 including a P well 12 without a mask;

masking the P well; and

forming a second gate structure 30 including an N well 14 in at least the N well.

10. Claim 38, as written, taught, and understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu (US '861).

Liu teaches a method comprising (see figures 1-6 and col. 1, line 20 to col. 4, line 35):

forming a first gate structure 3 including a P well 12;

masking the P well; and

forming a second gate structure 30 including an N well 14 using only one mask.

Liu further teaches that the first gate structure is formed to have a first conductivity using in-situ process in the substrate but Liu fails to teach that the first conductivity is introduced into the first gate structure by one blanket implantation as recited in present claim 38.

Gardner teaches a method for forming a CMOS device in which a doped polysilicon layer for forming gate structures is formed by blanket implantation. See figure 1A and col. 5, lines 25-40.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** form the first gate structure by blanket implantation because in doing so the use of masking is avoided.

11. Claim 56, as written, taught, and understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu (US '861).

Liu teaches a method comprising (see figures 1-6 and col. 1, line 20 to col. 4, line 35):

preparing a substrate 10,

forming a first gate structure 32; and

forming a second gate structure 30 including a NWELL using only one mask 22.

Liu teaches forming the first and second gate structures on a substrate but fails to teach that the substrate is doped n-type as recited in present claim 56.

However, the formation of gate structures or MOS devices on a substrate of n-type or p-type conductivity is well-known to one skilled in the semiconductor art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 703-308-1092. The examiner can normally be reached on M-F, 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4082 for regular communications and 703-746-4082 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Long Pham
Primary Examiner
Art Unit 2814

L. P.
May 28, 2003